Ex parte Katsura et al.

95-1248

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today:
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 39

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOYO KATSURA, HIDEO MAEJIMA,
and HIROSHI TAKEDA

Appeal No. 95-1248
Application 07/799,889[1]

HEARD: February 29, 1996

Before HARKCOM, Vice Chief Administrative Patent Judge, BARRETT and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 9-12 and 15-17.

References Relied on by the Examiner

Tabata et al. (Tabata)	4,785,296	Nov. 15, 1988
Watts et al. (Watts) (European Patent Application)	0,059,349	Sep. 8, 1982

[1] Application filed December 2, 1991. According to the appellants, it is a continuation of Application 07/198,067, filed May 24, 1988, now abandoned, and Application 06/626,992, filed July 2, 1984, now Patent No. 4,757,310.

The Rejection on Appeal

Claims 9-12 and 15-17 were finally rejected by the examiner as being unpatentable under 35 U.S.C. § 103 over the combined teachings of Tabata and Watts.

The Invention

The invention is directed to a system for displaying a plurality of display frames on a display screen. A memory stores the display data for each frame in separate regions corresponding to independent groups of addresses. The horizontal and vertical location, horizontal and vertical widths of each frame are stored and the system implements independent control over the location, width and height of each frame on the display screen. The system requires a timing processor responsive to clock signals from a clock for generating horizontal and vertical synchronization signals and other horizontal and vertical display timing signals for each frame of display data. The system further requires a display processor which acts in response to the synchronization and timing signals generated by the timing processor.

Independent claims 9 and 10 are representative:

> 9. A display controller for inputting and outputting a signal to and from a computer for storing information in a refresh memory in a drawing operation and for reading out the information stored in the refresh memory to display on a display region of a raster scan type display device in a display operation with the display operation being carried out in

synchronism with horizontal and vertical synchronizing signals in response to a clock comprising:

a timing processor responsive to clock signals from the clock including

means responsive to the clock for generating the horizontal and vertical synchronizing signals,

means for storing horizontal and vertical display positions and horizontal and vertical widths of each of a plurality of display frames; and

means for generating horizontal and vertical display timing signals for each of the plurality of display frames within the display region used for generating independent plural groups of display addresses of the plural display frames and for independently controlling the horizontal and vertical display positions and the horizontal and vertical widths of each of the display frames; and

a display processor for generating independent groups of display addresses in synchronism with the horizontal and vertical synchronizing signals and the horizontal and vertical display timing signals from said timing processor and feeding the display addresses to the refresh memory having a plurality of addressable memory regions of variable size for storing respectively the plurality of display frames.

10. A display controller for inputting and outputting a signal to and from a computer, for storing information in a refresh memory in a drawing operation and for reading out the information stored in the refresh memory for displaying on a display region of a raster type display device in a display operation with the display operation being carried out in synchronism with horizontal and vertical synchronizing signals in response to a clock comprising:

a timing processor responsive to clock signals from the clock for generating the horizontal and vertical synchronizing signals and for generating horizontal and vertical display timing signals determining horizontal and vertical positions and horizontal and vertical widths of each of a plurality

of display frames within the display region which are independently variable in size and position in the display region and

a display processor including

a plurality of storage means for storing a plurality of independent display starting addresses of the plurality of display frames prior to displaying each display frame in the display region,

means for sequentially renewing a plurality of groups of display addresses generated in response to the display starting addresses of the plurality of display frames in synchronism with each of the display timing signals from said timing processor for each of the display frames, and

means for providing the plurality of groups of the display addresses of the plurality of display frames to the refresh memory having a plurality of memory regions of variable size respectively corresponding to the plurality of display frames for reading data of the plurality of display frames.

Opinion

The rejection of claims 9-12 and 15-17 as being unpatentable over Tabata and Watts

The rejection of claims 9-12 and 15-17 as being unpatentable for obviousness over Tabata and Watts under 35 U.S.C. § 103 cannot be sustained.

The examiner erroneously determined (Answer at 2-3) that Tabata discloses the subject matter of claims 9-12 and 15-17, with the exception of a timing processor for generating horizontal and vertical synchronization signals. In addition to the "horizontal and vertical synchronization signals," the appellants' claims require the timing processor to generate horizontal and vertical display timing signals for each of the display frames in connection with either the generation of addresses or positioning of frames. Tabata does not disclose a timing processor which is responsive to clock signals and which generates horizontal and vertical display timing signals.

Moreover, because Tabata discloses no timing processor which generates the horizontal and vertical synchronization signals and the horizontal and vertical display timing signals, it does not disclose a display processor which acts in response to those synchronization and timing signals.

The appellants correctly stated (Br. at 6):

> Tabata is deficient with regard to teaching any of the details of how a display is generated by the display device 118 which displays the content of bit map memory 117 and further, the details of the display control unit 227 which is taught at col. 8, lines 49-51.

Watts does not make up for the deficiency of Tabata. The CRT controller 16 of Watts, shown in Watts' Figures 8a-8c, does

not include a timing processor which is responsive to clock signals from a clock for generating horizontal and vertical synchronization signals. As the appellants correctly noted (Br. at 9), while a clock signal CCLK is applied to a Memory CTL Buffers 162, there is no disclosed relationship between the element 162 and the vertical sync register 136. Note further that according to Watts at 18, the horizontal and vertical sync registers 132 and 136 are "free-running" counters.

Insofar as the means, in claims 9 and 15, for generating horizontal and vertical synchronization signals in response to clock signals is concerned, Watts does not disclose execution of the recited function, much less the same or equivalent structures, materials or acts which perform the function, as those in the appellants' specification. Inasmuch as the requirement, in claims 10 and 17, for the timing processor to generate other display timing signals in response to clock signals is concerned, we note that the state timing logic element 156 as shown in Watts' Figure 8c and described in Watts at 21 is not responsive to the applied clock signal CCLK.

Additionally, the system disclosed by Watts is also much different from that to which the claimed invention and the disclosed system of Tabata are directed. The system of Watts

does not support independent positioning of the plurality of frames and does not support independent control of the horizontal and vertical dimensions of the plurality of frames. Rather, in Watts, the entire display screen is partitioned and the plurality of frames are made to fit together like pieces in a puzzle, collectively occupying the entire screen. No overlap or superpositioning is contemplated. If the location or size of any frame is changed, that causes a corresponding change in the position and size of the other frames.

Because of its different nature, Watts does not store the horizontal and vertical positions and the horizontal and vertical width of all of the frames as is required by all of the appellants' claims. In Watts, the position and size of the frames are partly determinable from that of each other. The first frame begins at the first display position on the screen and the last frame ends at the last display position on the screen, with no gaps existing in between frames. If there is a split screen, the two screens are displayed side-by-side, extending to the full width of the display screen and terminating on the same row on the display.

Timing signal generation and corresponding memory addressing in Watts are implemented in light of certain fixed relationships

between the plurality of frames regarding the location and size of frames. For instance, the state timing logic 156 controls the register control logic 158 (Watts at 21) which in turn controls transfers from the memory address counter 144 which feeds a dedicated region 1 register 146 and a dedicated region 2 register 148 (Figure 8b). Regions 1 and 2 collectively constitute a split screen on the display and are predetermined to occupy the entire width of the screen and to terminate on the same row.

Even assuming that generation of the synchronization signals and other display timing signals as is required by the claims is disclosed in Watts, Watts' implementation is so bound up with the different nature of Watts' system that the disclosure would not have been regarded by one with ordinary skill in the art as being applicable in a system having independent control of the location and size of the frames. In that connection, we find that the component parts of Watts' CRT controller have no logically corresponding place in Tabata's disclosed system, and we find that it would not have been obvious to one with ordinary skill in the art just how the CRT controller of Watts can be adapted for use in a system like Tabata's, where the frame positions and sizes are independently controllable.

Conclusion

For the foregoing reasons, the rejection of claims 9-12 and 15-17 under 35 U.S.C. § 103 is reversed.

REVERSED

GARY V. HARKCOM
Vice Chief Administrative Patent Judge

LEE E. BARRETT
Administrative Patent Judge

JAMESON LEE
Administrative Patent Judge

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